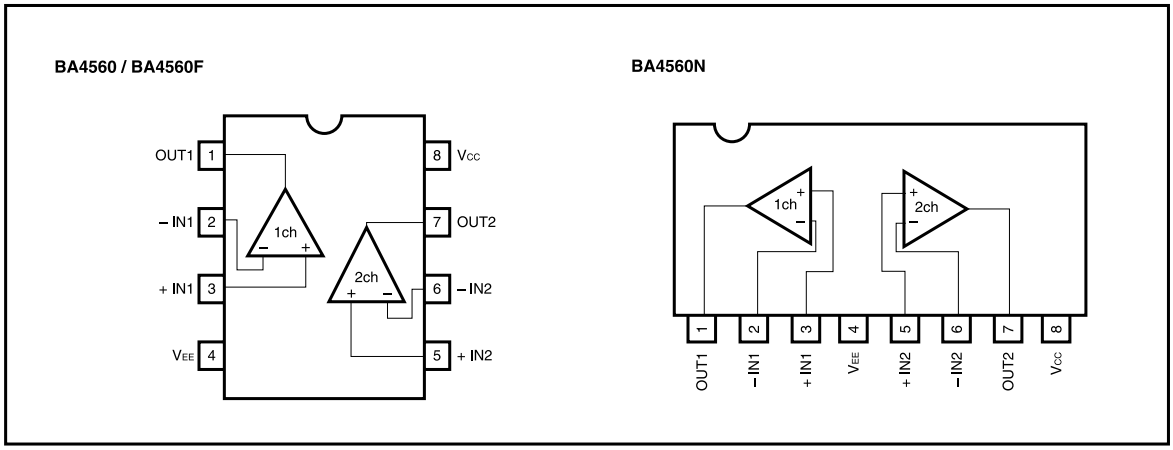
8. IC Block Diagrams

8-1 Main

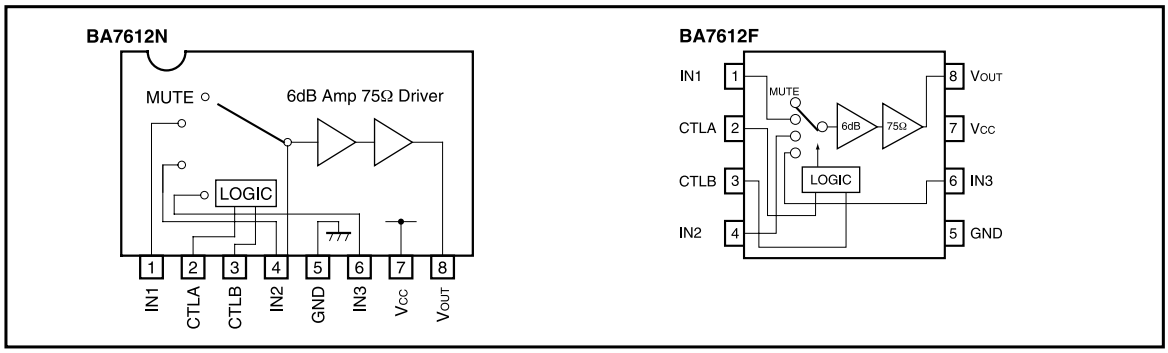
8-1-1. BA4560

●Block diagram



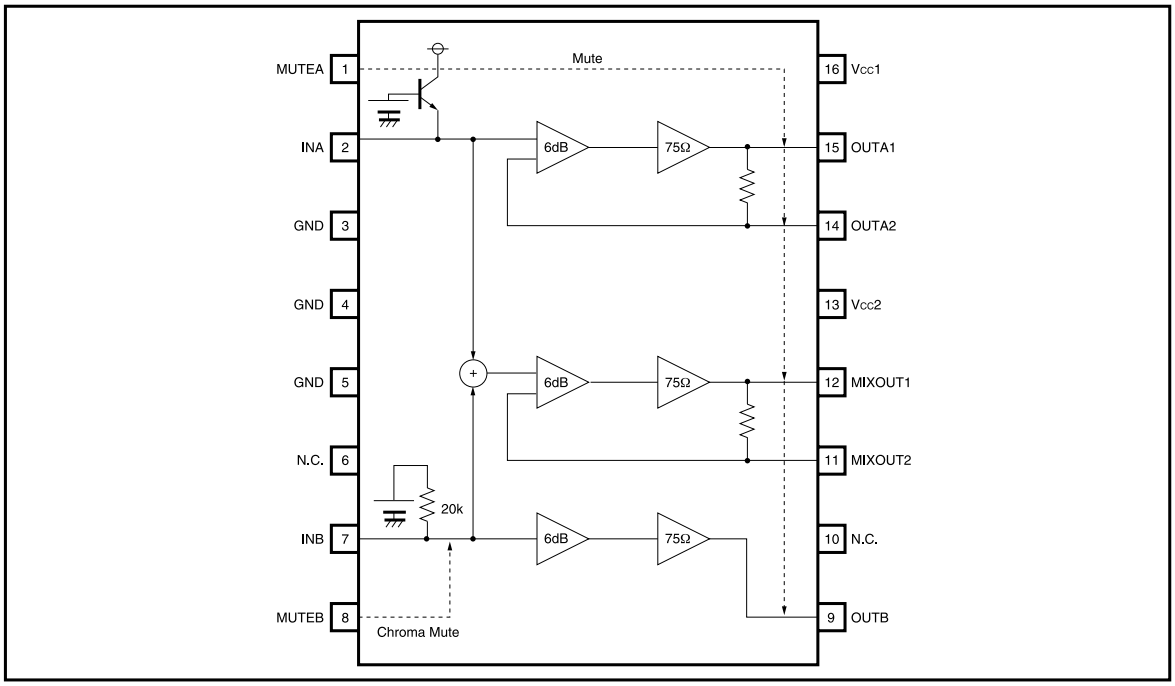
8-1-2. BA7612N

●Block diagram

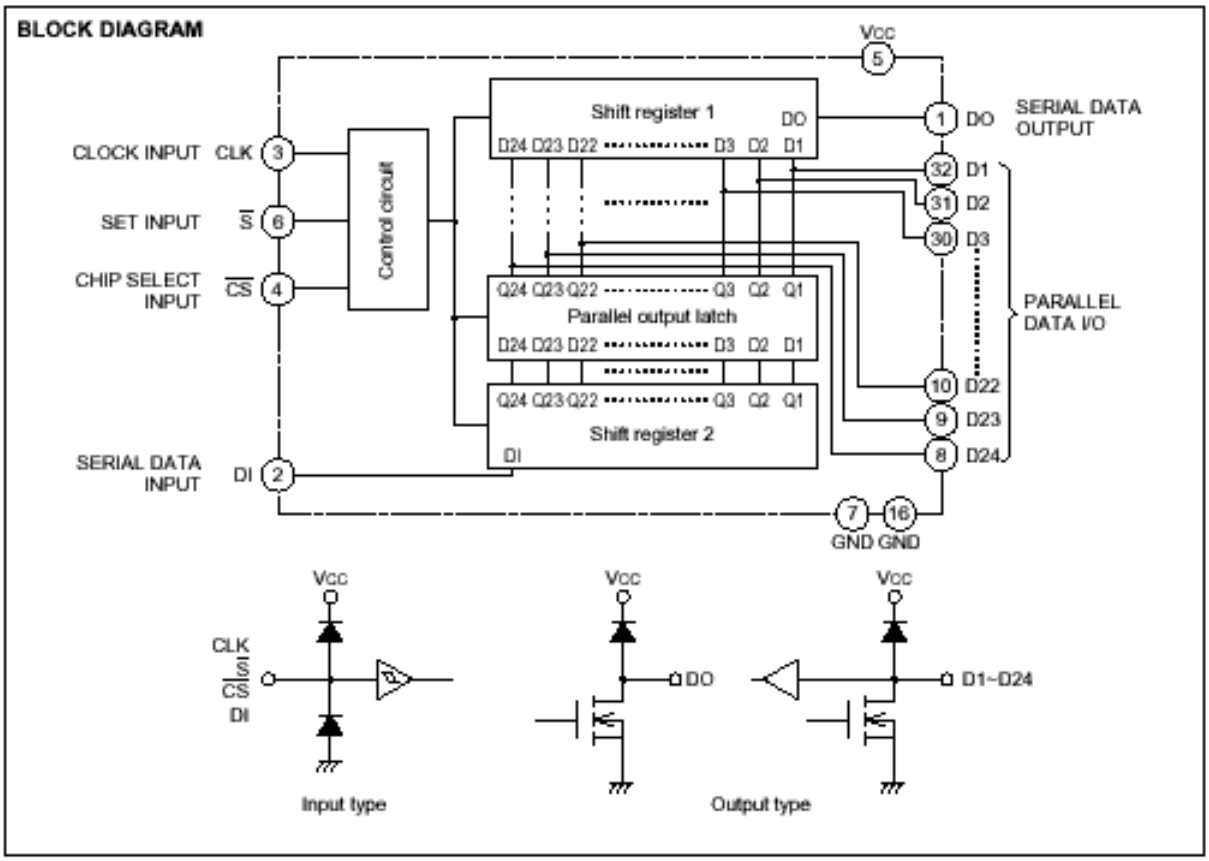


8-1-3. BA7665FS

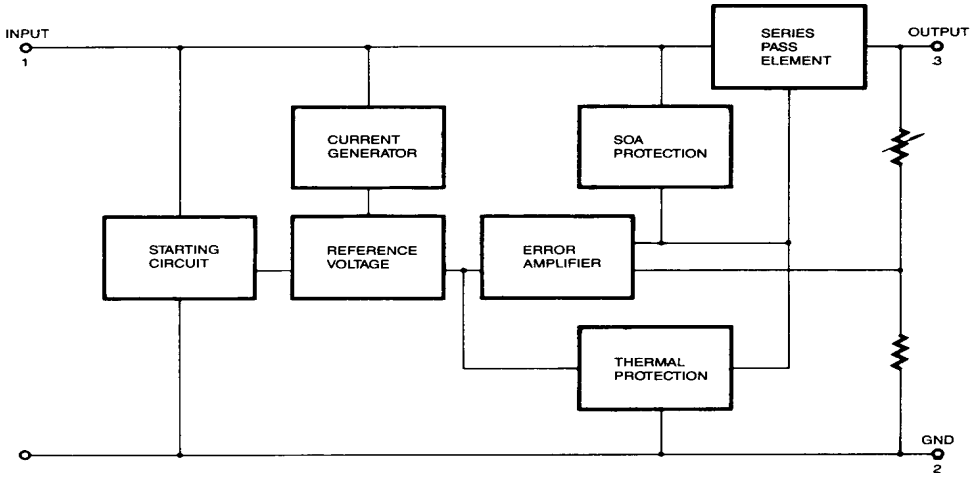
●Block diagram



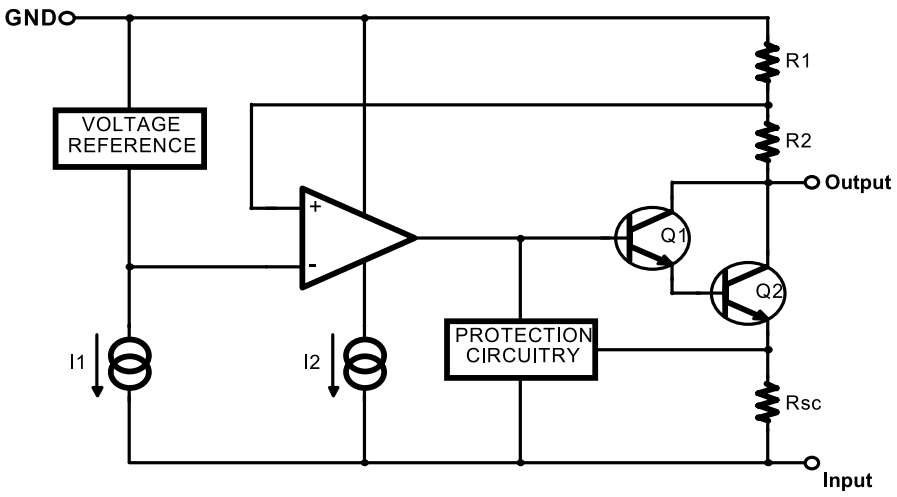
8-1-4. M66010FP



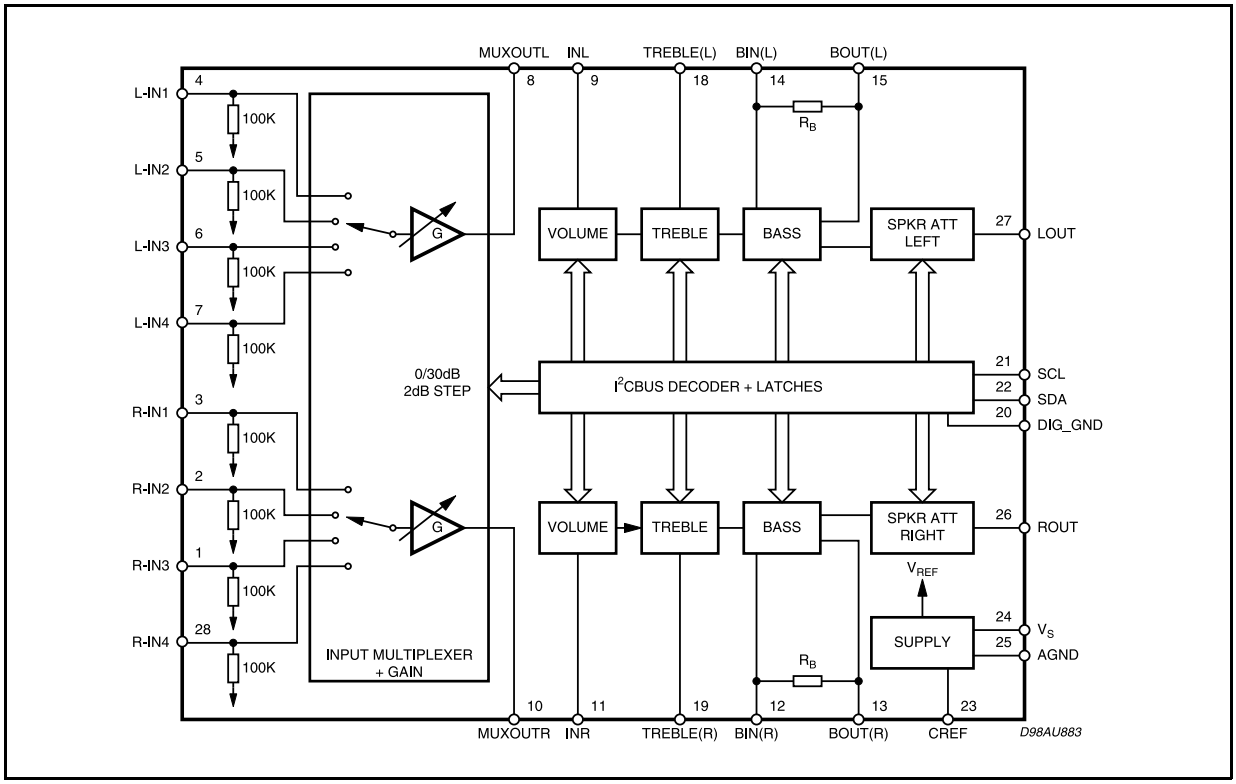
8-1-5. KA7805/ 7808/ 7812



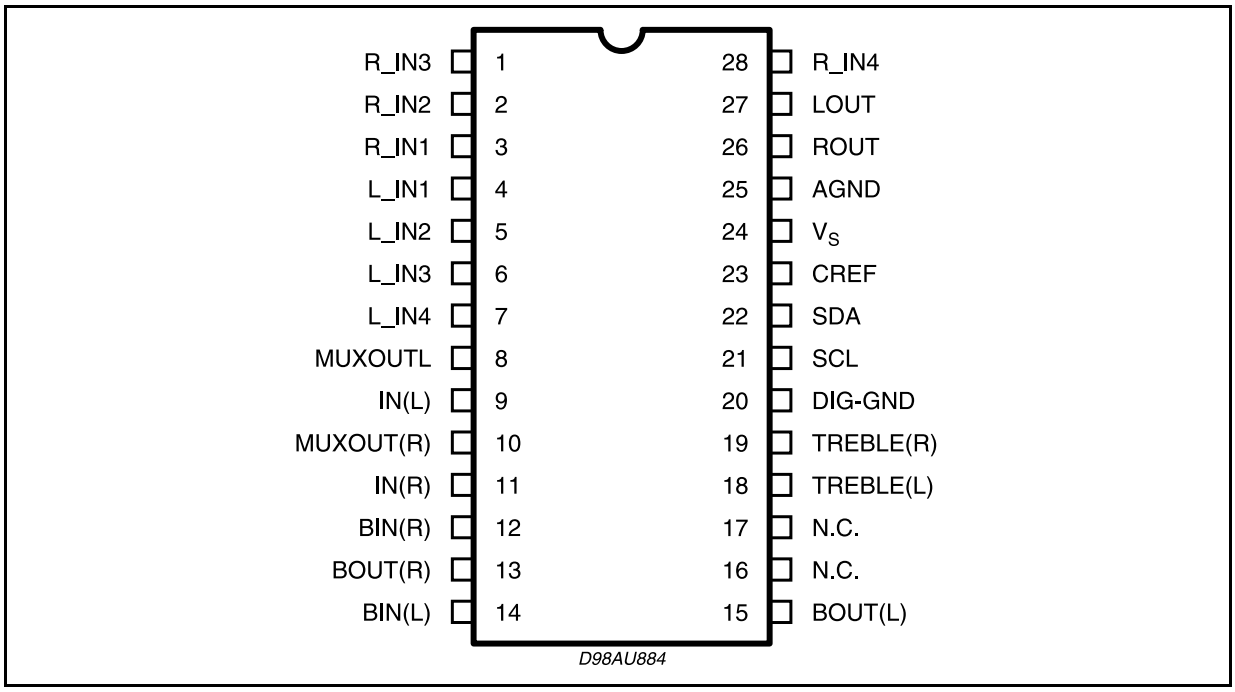
8-1-6. KA7912



BLOCK DIAGRAM



PIN CONNECTION (Top view)



ES60X8 PINOUT DIAGRAM

The identical device pinouts for the ES6008, ES6018, ES6028 and ES6038 are shown in Figure

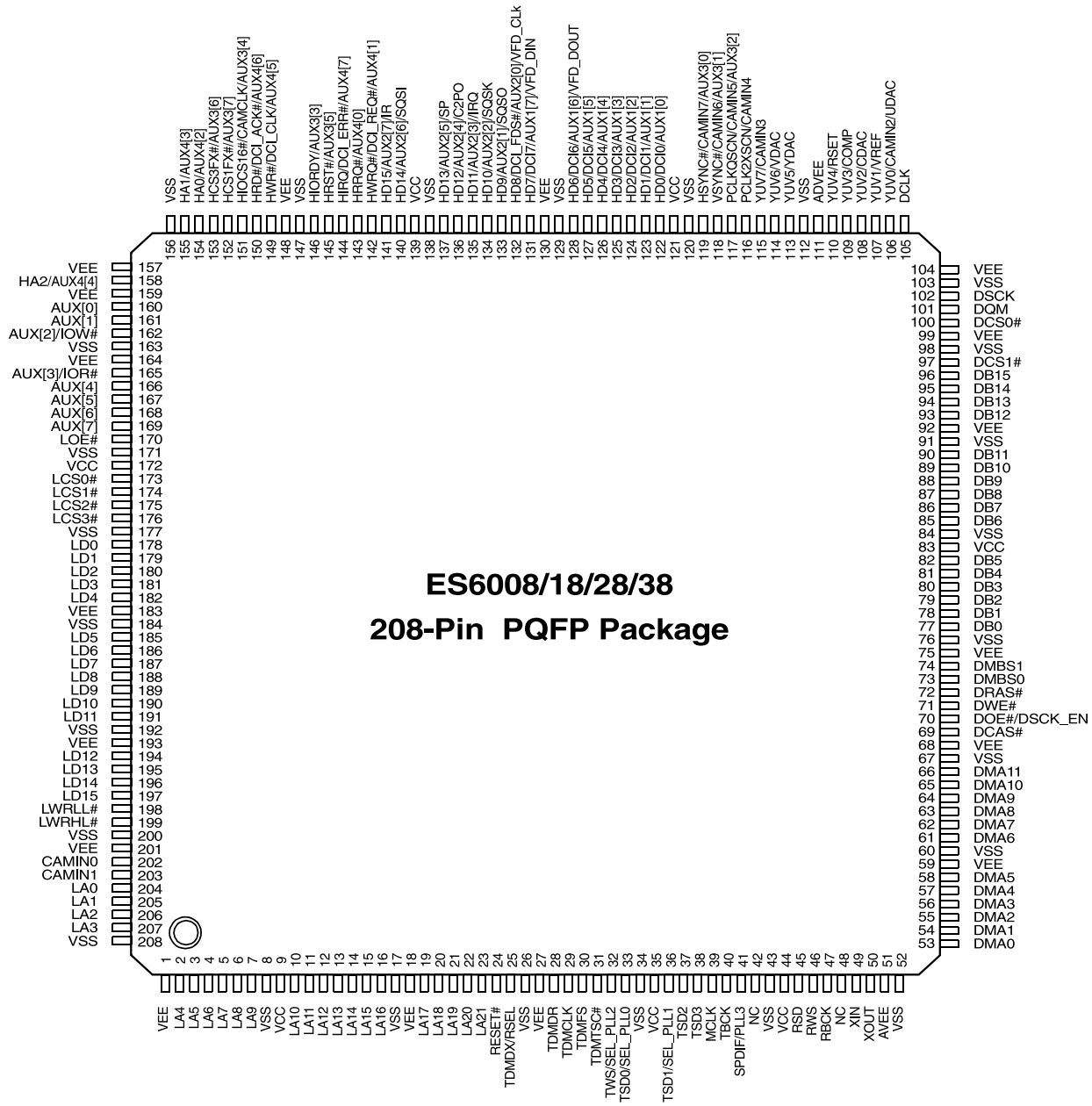


Figure ES60x8 Pinout

ES60X8 PIN DESCRIPTION

Table 1 lists the identical pin descriptions for the ES6008, ES6018, ES6028 and ES6038.

Table 1 ES60x8 Pin Description

<table>
<tr><th>Name</th><th>Number</th><th>I/O</th><th>Definition</th></tr>
<tr><td>VEE</td><td>1,18, 27, 59, 68, 75, 92, 99, 104, 130, 148, 157, 159, 164, 183, 193, 201</td><td>I</td><td>I/O power supply.</td></tr>
<tr><td>VSS</td><td>8, 17, 26, 34, 43, 52, 60, 67, 76, 84, 91, 98, 103, 112, 120, 129, 138, 147, 156, 163, 171, 177, 184, 192, 200, 208</td><td>I</td><td>Ground.</td></tr>
<tr><td>LA[21:0]</td><td>23:19, 16:10, 7:2, 207:204</td><td>O</td><td>Device address output.</td></tr>
<tr><td>VCC</td><td>9, 35, 44, 83, 121, 139, 172</td><td>I</td><td>Core power supply.</td></tr>
<tr><td>RESET#</td><td>24</td><td>I</td><td>Reset input, active low.</td></tr>
<tr><td>TDMDX</td><td rowspan="2">25</td><td>O</td><td>TDM transmit data.</td></tr>
<tr><td>RSEL</td><td>I</td><td>ROM Select.
<table>
<tr><th>RSEL</th><th>Selection</th></tr>
<tr><td>0</td><td>16-bit OM R</td></tr>
<tr><td>1</td><td>8-bit ROM</td></tr>
</table></td></tr>
<tr><td>TDMDR</td><td>28</td><td>I</td><td>TDM receive data.</td></tr>
<tr><td>TDMCLK</td><td>29</td><td>I</td><td>TDM clock input.</td></tr>
<tr><td>TDMFS</td><td>30</td><td>I</td><td>TDM frame sync.</td></tr>
<tr><td>TDMTSC#</td><td>31</td><td>O</td><td>TDM output enable.</td></tr>
<tr><td>TWS</td><td rowspan="2">32</td><td>O</td><td>Audio transmit frame sync.</td></tr>
<tr><td>SEL_PLL2</td><td>I</td><td>System and DSCK output clock frequency selection is made at the rising edge of RESET#. The matrix below lists the available clock frequencies and their respective PLL bit settings.
<table>
<tr><th>SEL_PLL2</th><th>SEL_PLL1</th><th>SEL_PLL0</th><th>Clock Type</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>VCO off.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DCLK</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Bypass mode</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DCLK x 2</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>DCLK x 4.5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>DCLK x 3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>DCLK x 3.5z</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>DCLK x 4</td></tr>
</table></td></tr>
<tr><td>TSD0</td><td rowspan="2">33</td><td>O</td><td>Audio transmit serial data port 0.</td></tr>
<tr><td>SEL_PLL0</td><td>I</td><td>Refer to the description and matrix for SEL_PLL2 pin 32.</td></tr>
<tr><td>TSD1</td><td rowspan="2">36</td><td>O</td><td>Audio transmit serial data port 1.</td></tr>
<tr><td>SEL_PLL1</td><td>I</td><td>Refer to the description and matrix for SEL_PLL2 pin 32.</td></tr>
<tr><td>TSD[2]</td><td>37</td><td>O</td><td>Audio transmit serial data output 2.</td></tr>
<tr><td>TSD[3]</td><td>38</td><td>O</td><td>Audio transmit serial data output 3.</td></tr>
</table>

Table 1 ES60x8 Pin Description (Continued)

<table>
<tr><th>Name</th><th>Number</th><th>I/O</th><th>Definition</th></tr>
<tr><td>MCLK</td><td>39</td><td>I/O</td><td>Audio master clock for audio DAC.</td></tr>
<tr><td>TBCK</td><td>40</td><td>O</td><td>Audio transmit bit clock.</td></tr>
<tr><td>SPDIF</td><td rowspan="2">41</td><td>O</td><td>S/PDIF output.</td></tr>
<tr><td>SEL_PLL3</td><td>I</td><td>Clock source select.
<table>
<tr><th>SEL_PLL3</th><th>Clock Source</th></tr>
<tr><td>0</td><td>Crystal oscillator</td></tr>
<tr><td>1</td><td>DCLK input</td></tr>
</table></td></tr>
<tr><td>NC</td><td>42, 48</td><td></td><td>No connect pins. Leave open.</td></tr>
<tr><td>RSD</td><td>45</td><td>I</td><td>Audio receive serial data.</td></tr>
<tr><td>RWS</td><td>46</td><td>I</td><td>Audio receive frame sync.</td></tr>
<tr><td>RBCK</td><td>47</td><td>I</td><td>Audio receive bit clock.</td></tr>
<tr><td>XIN</td><td>49</td><td>I</td><td>Crystal input.</td></tr>
<tr><td>XOUT</td><td>50</td><td>O</td><td>Crystal output.</td></tr>
<tr><td>AVEE</td><td>51</td><td>I</td><td>Analog power for PLL.</td></tr>
<tr><td>DMA[11:0]</td><td>66:61, 58:53</td><td>O</td><td>DRAM address bus [11:0].</td></tr>
<tr><td>DCAS#</td><td>69</td><td>O</td><td>DRAM column address strobe.</td></tr>
<tr><td>DOE#</td><td rowspan="2">70</td><td>O</td><td>DRAM output enable.</td></tr>
<tr><td>DSCK_EN</td><td>O</td><td>DRAM clock enable.</td></tr>
<tr><td>DWE#</td><td>71</td><td>O</td><td>DRAM write enable.</td></tr>
<tr><td>DRAS#</td><td>72</td><td>O</td><td>DRAM row address strobe.</td></tr>
<tr><td>DMBS0</td><td>73</td><td>O</td><td>SDRAM bank select 0.</td></tr>
<tr><td>DMBS1</td><td>74</td><td>O</td><td>SDRAM bank select 1.</td></tr>
<tr><td>DB[15:0]</td><td>96:93, 90:85, 82:77</td><td>I/O</td><td>DRAM data bus [15:0].</td></tr>
<tr><td>DCS[1:0]#</td><td>97,100</td><td>O</td><td>SDRAM chip select [1:0].</td></tr>
<tr><td>DQM</td><td>101</td><td>O</td><td>Data input/output mask.</td></tr>
<tr><td>DSCK</td><td>102</td><td>O</td><td>Output clock to SDRAM.</td></tr>
<tr><td>DCLK</td><td>105</td><td>I</td><td>27 MHz clock input to PLL.</td></tr>
<tr><td>YUV0</td><td rowspan="3">106</td><td>O</td><td>YUV0 pixel output data.</td></tr>
<tr><td>CAMIN2</td><td>I</td><td>Camera input 2.</td></tr>
<tr><td>UDAC</td><td>O</td><td>Video DAC output.
<table>
<tr><th>Mode</th><th>YDAC</th><th>UDAC</th><th>VDAC</th><th>CDAC</th></tr>
<tr><td>A</td><td>Y</td><td>C</td><td>Composite</td><td>C</td></tr>
<tr><td>B</td><td>Y</td><td>Composite</td><td>Composite</td><td>C</td></tr>
<tr><td>C</td><td>Y</td><td>U</td><td>Composite</td><td>V</td></tr>
<tr><td>D</td><td>Y</td><td>U</td><td>C</td><td>V</td></tr>
</table>
Y: Luma component for YUV and Y/C processing.
C: Chrominance signal for Y/C processing.
U: Chrominance component signal for YUV mode.
V: Chrominance component signal for YUV mode.</td></tr>
</table>

Table 1 ES60x8 Pin Description (Continued)

Name	Number	I/O	Definition
YUV1	107	O	YUV1 pixel output data.
VREF		I	Internal voltage reference to video DAC. Bypass to ground with 0.1 F capacitor.
YUV2	108	O	YUV2 pixel output data.
CDAC		O	Video DAC output. Refer to description and matrix for UDAC pin 106.
YUV3	109	O	YUV3 pixel output data.
COMP		I	Compensation input. Bypass to ADVEE with 0.1 F capacitor.
YUV4	110	O	YUV4 pixel output data.
RSET		I	DAC current adjustment resistor input.
ADVEE	111	I	Analog power for video DAC.
YUV5	113	O	YUV5 pixel output data.
YDAC		O	Video DAC output. Refer to description and matrix for UDAC pin 106.
YUV6	114	O	YUV6 pixel output data.
VDAC		O	Video DAC output. Refer to description and matrix for UDAC pin 106.
YUV7	115	O	YUV7 pixel output data.
CAMIN3		I	Camera YUV 3.
PCLK2XSCN	116	I/O	27-MHz video output pixel clock.
CAMIN4		I	Camera YUV 4.
PCLKQSCN	117	O	13.5-MHz video output pixel clock.
CAMIN5		I	Camera YUV 5.
VSYNC#	118	I/O	Vertical sync, active low.
CAMIN6		I	Camera YUV 6.
HSYNC#	119	I/O	Horizontal sync, active low.
CAMIN7		I	Camera YUV 7.
HD[5:0]	127:122	I/O	Host data I/O [5:0].
DCI[5:0]		I/O	DVD channel data I/O [5:0].
AUX1[5:0]		I/O	Aux1 data I/O [5:0].
HD[6]	128	I/O	Host data I/O [6].
DCI[6]		I/O	DVD channel data I/O [6].
AUX1[6]		I/O	Aux1 data I/O [6].
VFD_DOUT		I	VFD data output.
HD[7]	131	I/O	Host data I/O [7].
DCI[7]		I/O	DVD channel data I/O [7].
AUX1[7]		I/O	Aux1 data I/O [7:0].
VFD_DIN		I	VFD data input.
HD[8]	132	I/O	Host data bus 8.
DCI_FDS#		I/O	DVD input sector start.
AUX2[0]		I/O	Aux2 data I/O 0.
VFD_CLK		I	VFD clock input.
HD[9]	133	I/O	Host data bus line 9.
AUX2[1]		I/O	Aux2 data I/O [1] when selected.
SQSQ		I	Subcode-Q data.
HD[10]	134	I/O	Host data bus line10.
AUX2[2]		I/O	Aux2 data I/O [2] when selected.
SQSK		I	Subcode-Q clock.

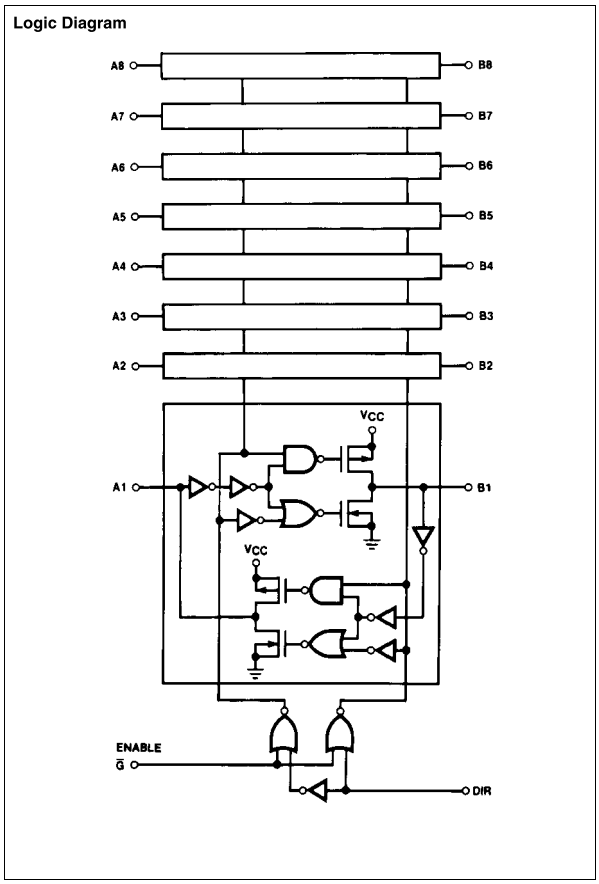
Table 1 ES60x8 Pin Description (Continued)

Name	Number	I/O	Definition
HD[11]	135	I/O	Host data bus line11.
AUX2[3]		I/O	Aux2 data I/O [3] when selected.
IRQ		O	IRQ output.
HD[12]	136	I/O	Host data bus line12.
AUX2[4]		I/O	Aux2 data I/O [4] when selected.
C2PO		I	C2PO error correction flag from CD-ROM.
HD[13]	137	I/O	Host data bus line13.
AUX2[5]		I/O	Aux2 data I/O [5] when selected.
SP		I	16550 UART serial port input.
HD[14]	140	I/O	Host data bus line14.
AUX2[6]		I/O	Aux2 data I/O [6] when selected.
SQSI		I	Subcode-Q sync.
HD[15]	141	I/O	Host data bus line15.
AUX2[7]		I/O	Aux2 data I/O [7] when selected.
IR		I	IR remote control input.
HWRQ#	142	O	Host write request.
DCI_REQ#		O	DVD control interface request.
AUX4[1]		I/O	Aux4 data I/O 1.
HRRQ#	143	O	Host read request.
AUX4[0]		I/O	Aux4 data I/O 0.
HIRQ	144	I/O	Host interrupt.
DCI_ERR#		I/O	DVD channel data error.
AUX4[7]		I/O	Aux4 data I/O 7.
HRST#	145	O	Host reset.
AUX3[5]		I/O	Aux3 data I/O 5.
HIORDY	146	I	Host I/O ready.
AUX3[3]		I/O	Aux3 data I/O 3.
HWR#	149	I/O	Host write.
DCI_CLK		I/O	DVD channel data clock.
AUX4[5]		I/O	Aux4 data I/O 5.
HRD#	150	O	Host ead.
DCI_ACK#		O	DVD channel data valid.
AUX4[6]		I/O	Aux4 data I/O 6.
HIOCS16#	151	I	Device 16-bit data transfer.
CAMCLK		I	Camera port pixel clock input.
AUX3[4]		I/O	Aux3 data I/O 4.
HCS1FX#	152	O	Host select 1.
AUX3[7]		I/O	Aux3 data I/O 7.
HCS3FX#	153	O	Host select 3.
AUX3[6]		I/O	Aux3 data I/O 6.
HA[2:0]	158, 155:154	I/O	Host address bus.
AUX4[4:2]		I/O	Aux4 data I/Os [4:2].
AUX[1:0]	160	I/O	Auxiliary ports 1:0.

Table 1 ES60x8 Pin Description (Continued)

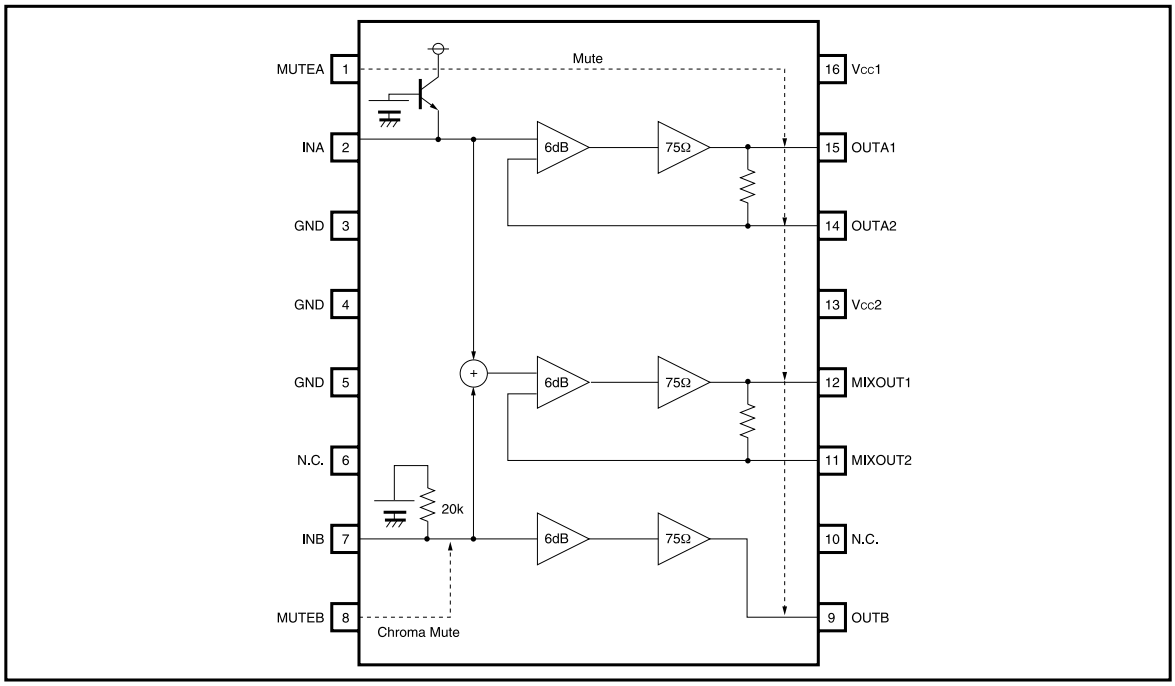
Name	Number	I/O	Definition
AUX[2]	162	I/O	Auxiliary port 2.
IOW#		O	I/O Write strobe.
AUX[3]	165	I/O	Auxiliary port 3.
IOR#		O	I/O Read strobe.
AUX[7:3]	169:166	I/O	Auxiliary ports 7:3.
LOE#	170	O	Device output enable.
LCS[3:0]#	176:173	O	Chip select [3:0].
LD[15:0]	197:194, 191:185, 182:178	I/O	EPROM device data bus.
LWRLL#	198	O	Device low-byte write enable.
LWRHL#	199	O	Device high-byte write enable.
CAMIN0	202	I	Camera YUV 0.
CAMIN1	203	I	Camera YUV 1.

8-2-2. 74HCT245

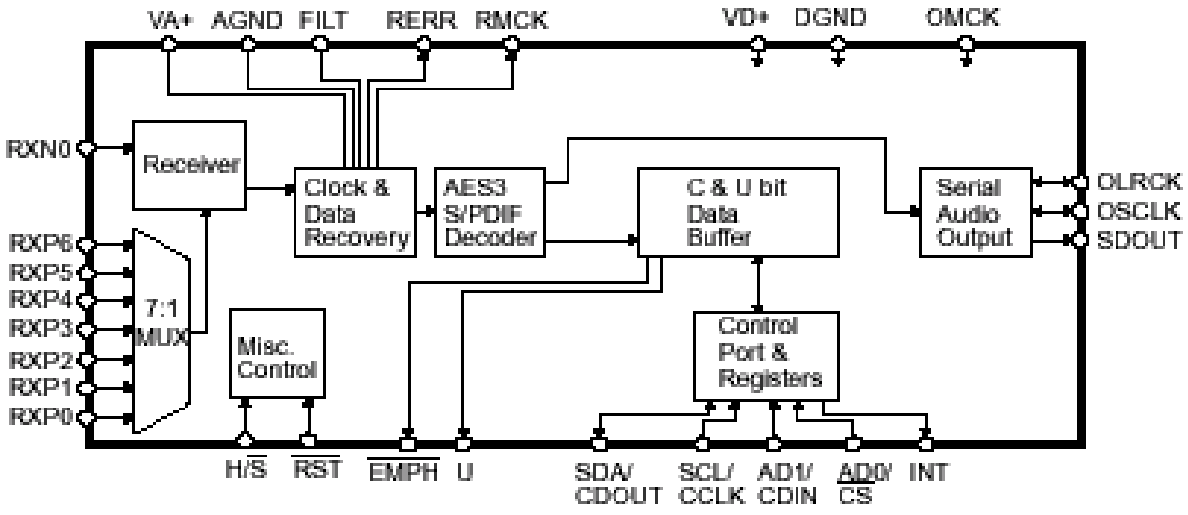


8-2-3. BA7665FS

●Block diagram

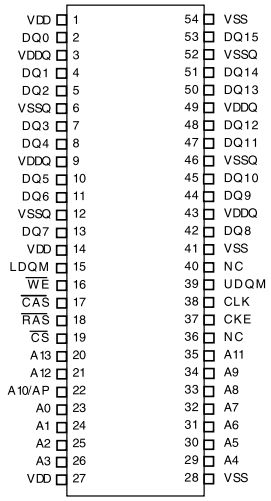


8-2-4. CS8415

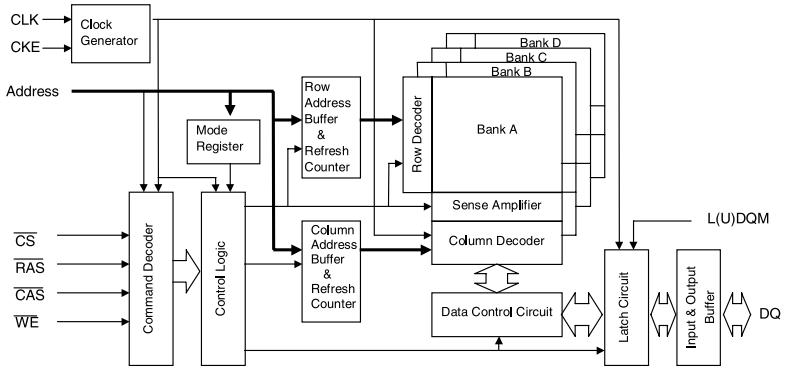


PIN ASSIGNMENT

Top View



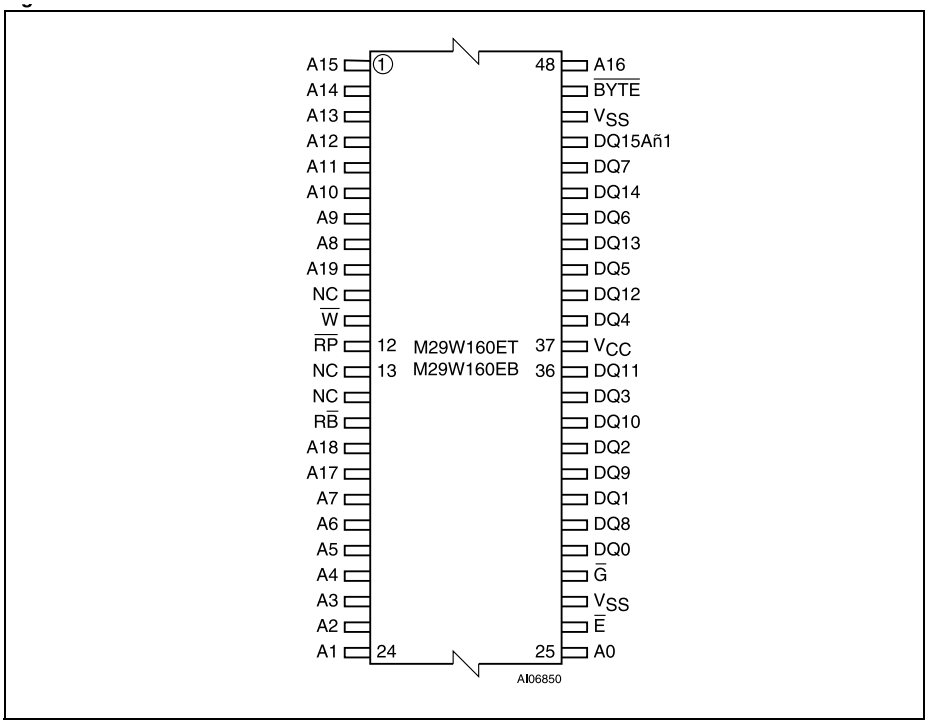
FUNCTIONAL BLOCK DIAGRAM



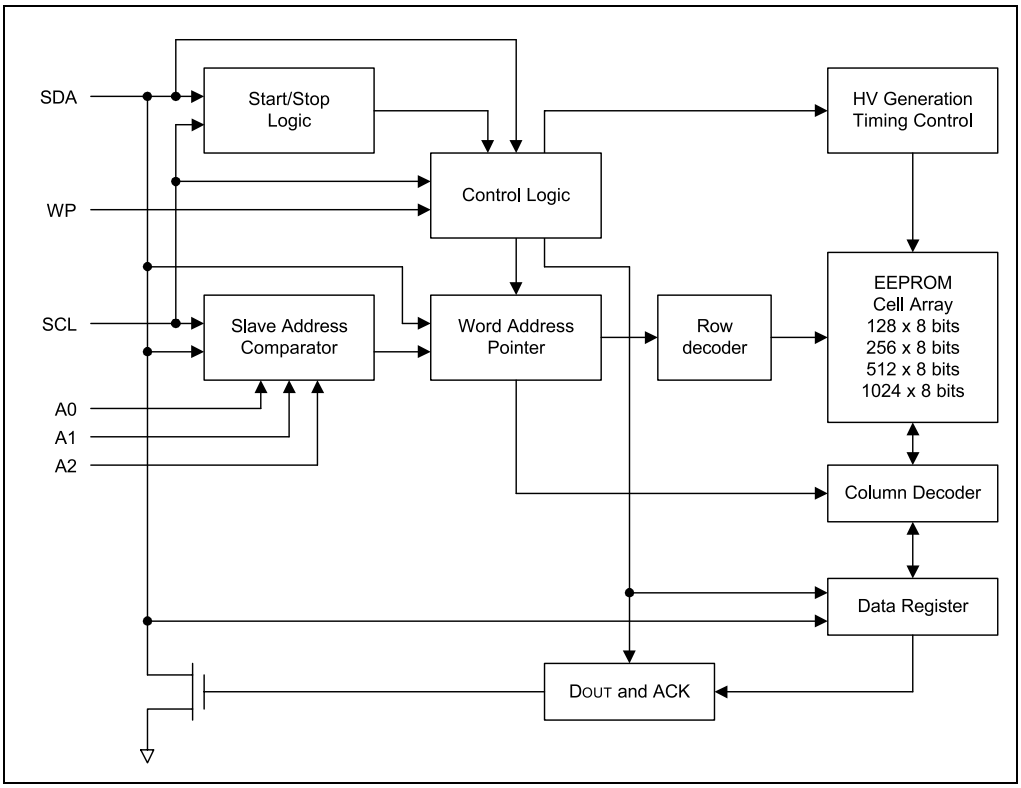
PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	System Clock	Active on the positive going edge to sample all inputs
$\overline{CS}$	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK , CKE and L(U)DQM
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row / column address are multiplexed on the same pins. Row address : RA0~RA11, column address : CA0~CA7
A12 , A13	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column address on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	Data Input / Output Mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ0 ~ DQ15	Data Input / Output	Data inputs / outputs are multiplexed on the same pins.
VDD / VSS	Power Supply / Ground	Power and ground for the input buffers and the core logic.
VDDQ / VSSQ	Data Output Power / Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC	No Connection	This pin is recommended to be left No Connection on the device.

8-2-6. M29W160E



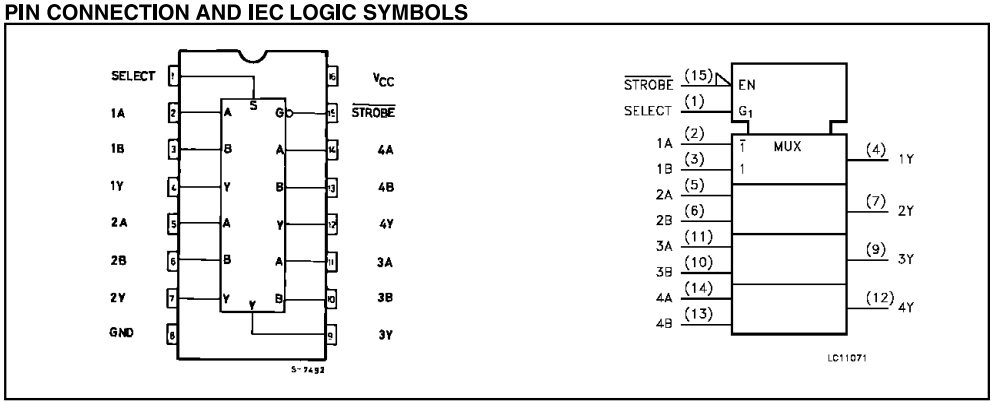
8-2-7. S524C20D21_20D41



S524C20D11/20D21/80D41/80D81 Block Diagram

8-2-8. STM_74LCX157

PIN CONNECTION AND IEC LOGIC SYMBOLS

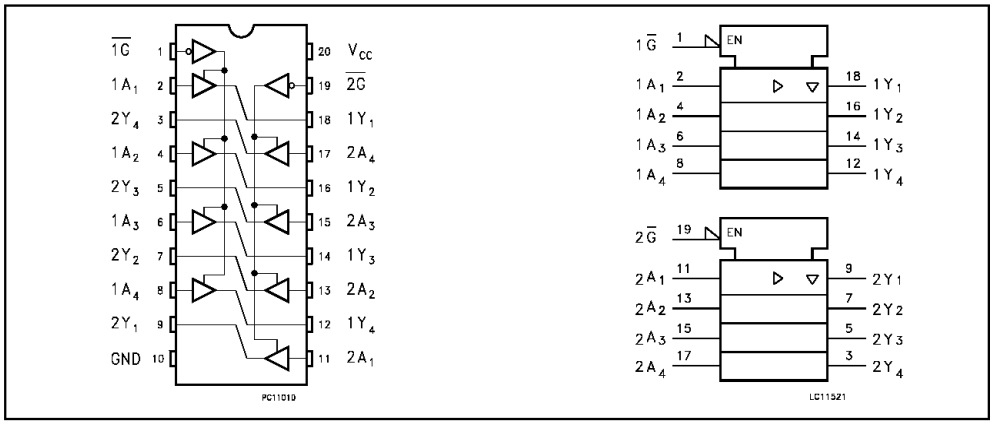


PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	SELECT	Common Data Select Inputs
2, 5, 11, 14	1A to 4A	Data Inputs From Source A
3, 6, 10, 13	1B to 4B	Data Inputs From Source B
4, 7, 9, 12	1Y to 4Y	Multiplexer Outputs
15	STROBE	Strobe Input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

8-2-9. STM_74LCX244

PIN CONNECTION AND IEC LOGIC SYMBOLS



PIN DESCRIPTION

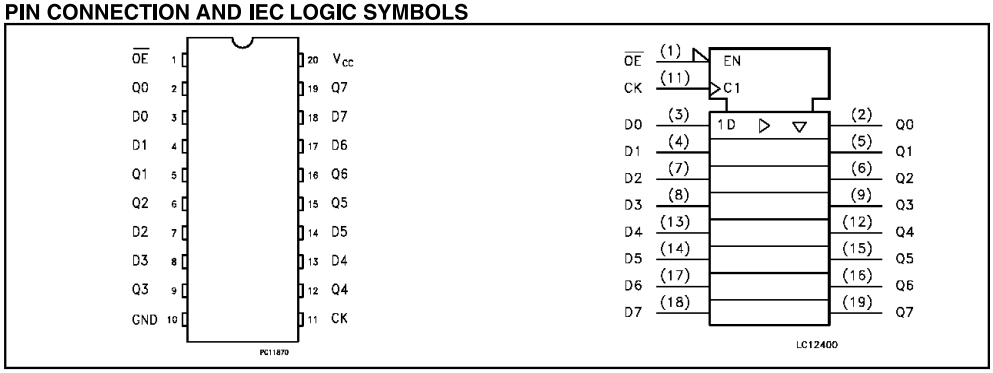
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	2Y1 to 2Y4	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	1Y1 to 1Y4	Data Outputs
19	$\overline{2G}$	Output Enable Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUT		OUTPUT
$\overline{G}$	An	Yn
L	L	L
L	H	H
H	X	Z

X : Don't Care
Z : High Impedance

PIN CONNECTION AND IEC LOGIC SYMBOLS



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State Output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	3-State Outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CK	Clock Input (LOW to HIGH edge triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

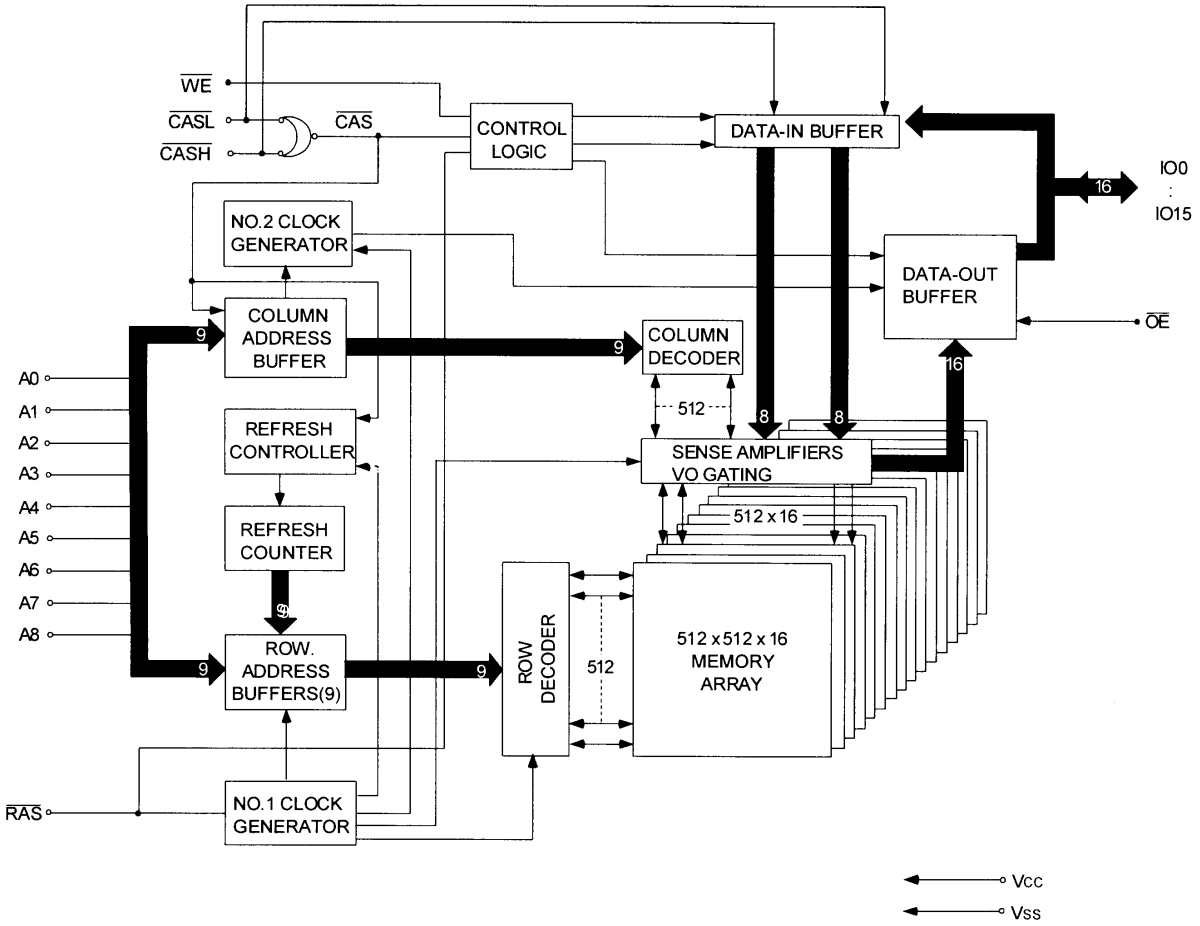
TRUTH TABLE

INPUT			OUTPUT
$\overline{OE}$	CK	D	Q
H	X	X	Z
L	↓	X	NO CHANGE
L	↑	L	L
L	↑	H	H

X : Don't Care
Z : High Impedance

8-3-1. M11B416256A

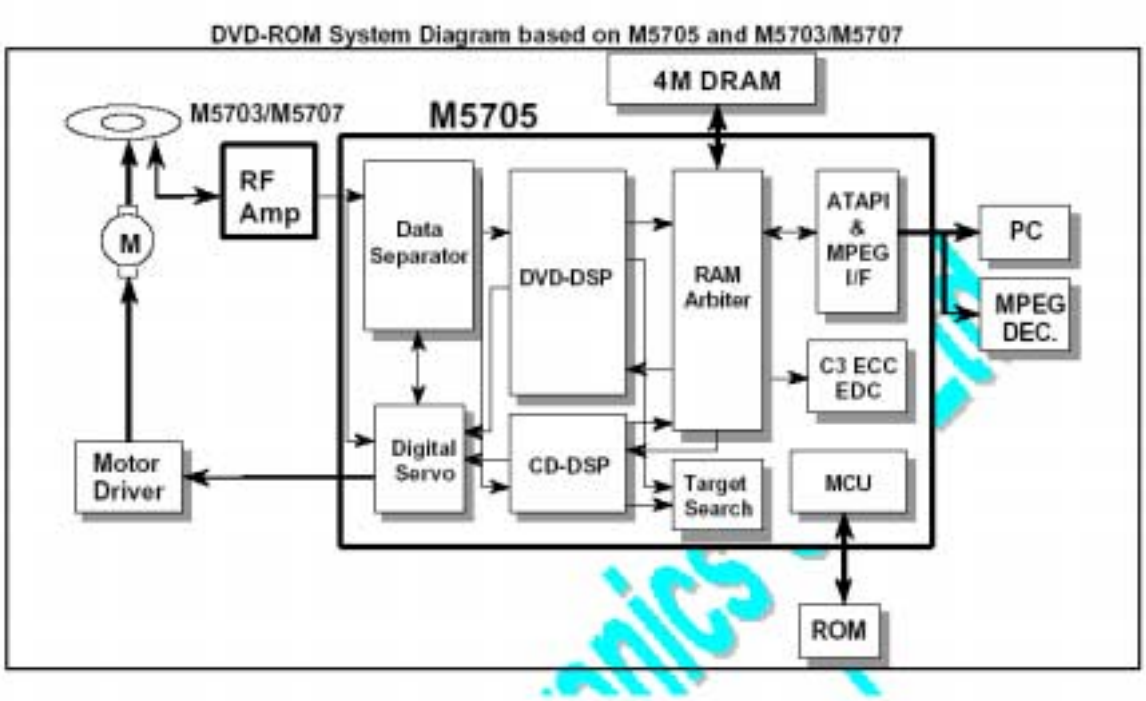
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

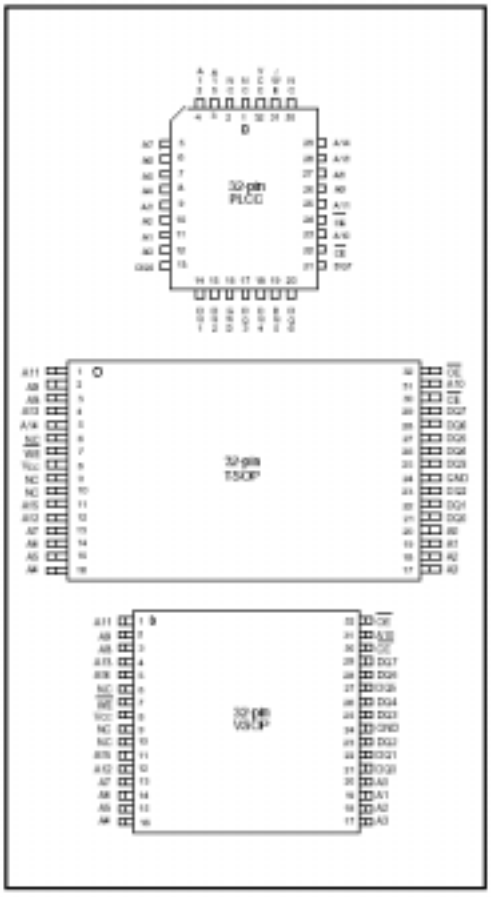
PIN NO.	SYM.	TYPE	DESCRIPTION
16~19,22~26	A0~A8	Input	Address Input
14	$\overline{RAS}$	Input	Row Address Strobe
28	$\overline{CASH}$	Input	Column Address Strobe/Upper Byte Control
29	$\overline{CASL}$	Input	Column Address Strobe/Lower Byte Control
13	$\overline{WE}$	Input	Write Enable
27	$\overline{OE}$	Input	Output Enable
2~5,7~10,31~34,36~39	I/O0 ~ I/O15	Input/Output	Data Input/Output
1,6,20	Vcc	Supply	Power, 5V
21,35,40	Vss	Ground	Ground
11,12,15,30	NC	-	No Connect

8-3-2. M5705

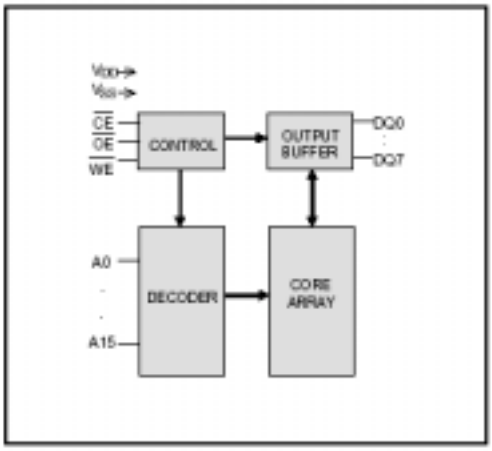


8-3-3. W29EE512F1

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0–A15	Address Inputs
DQ0–DQ7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
VCC	Power Supply
GND	Ground
NC	No Connection